

A Low Power Hybrid DCO Using Three Transistor (3-T) XNOR Gate, CMOS and Pseudo-NMOS Inverter

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Abstract: This research article presents a comprehensive investigation of three-bit hybrid-digitally controlled ring oscillator (HDCRO) implemented with TSMC 90nm CMOS technology. The hybrid circuit HDCRO comprises of three distinct delay stages, namely XNOR-based inverter, a CMOS inverter, and a Pseudo-NMOS inverter, all of which have been designed utilizing an inversion MOS varactor (IMOS). Furthermore, the investigation explores the output frequency variation in the load element of the HDCRO by adjusting the capacitance of the digitally controlled MOS varactors. This frequency variation occurs as a result of changing the digital control bits of the MOS varactors at a supply voltage of 0.7 V. The proposed HDCRO demonstrates an oscillation frequency range of 2.558 GHz to 2.649 GHz, with power consumption varying from 3.638 mW to 1.046 mW, and phase noise from -68.070 dB@1 MHz to -67.654 dB@1 MHz relative to the central oscillation frequency. Moreover, by applying a supply voltage variation between 0.5 V and 1 V, a wider frequency tuning range of 1.238 GHz to 4.438 GHz is achieved. This extended tuning range exhibits power consumption variation from 2.785 μ W to 54.66 mW, and phase noise from -68.812 dB@1 MHz to -65.445 dB@1 MHz relative to the central oscillation frequency. In summary, this study presents a novel HDCRO architecture that demonstrates excellent performance in terms of frequency range, power consumption and phase noise. The proposed design offers advantages of high speed, low-power and good frequency range; thus has a promising prospect of application in high-performance integrated circuits.

Keywords: Hybrid Digitally Controlled Oscillator, MOS varactor, Phase noise, Delay stage, Pseudo-NMOS inverter.

1. Introduction

An oscillator is an electronic circuit designed to take a DC signal as input and generate a periodic, repetitive, and continuous alternating waveform (AC) with the desired frequency, ranging from a few hertz (Hz) to hundreds of gigahertz (GHz). The oscillator's output can take the form of a sinusoidal waveform or non-sinusoidal signals such as square waves and triangular waves. It serves as a device for generating oscillatory voltages or currents without the need for mechanical components. There are many types of oscillators which can be digitally or analogously controlled [1-6]. A specialized type of controlled system known as a phase-locked loop (PLL) is engineered to uphold a constant phase relationship between the input and output signals. PLLs are available in diverse variants, such as Analog PLL (APLL), Digital PLL (DPLL), All-Digital PLL (ADPLL), and Software PLL (SPLL). The integral part of the PLL is the VCO. It is an oscillator which employs external voltage to the frequency of output signal.

The frequency of output signal can be varied by varying the value of passive components. As the control voltage increases, the diode's capacitance decreases, thereby raising the oscillation frequency. The various specifications of VCO's are tuning range, tuning gain (tuning sensitivity), supply pushing, load pulling, and spectral purity, which can be analyzed in either the time domain or frequency domain. Voltage-Controlled Oscillators (VCOs) are extensively utilized in CMOS technology, and as a result, the CMOS scaling continually advances, leading to downsizing or deep-submicrometer scaling. However, the implementation of VCO designs in CMOS deep-submicrometer technology poses significant challenges. This issue of VCO is due to the nonlinear behavior of frequency versus voltage. So, it is susceptible to noise, ground supply and high-power consumption etc. Thus, it is very problematic to attain a frequency tuning of low voltage for deep-submicrometer CMOS by using VCO. To address the challenges encountered in deep submicrometer CMOS technology, researchers and manufacturers adopt a digital-intensive approach to effectively control the frequency of oscillation. Consequently, the Voltage-Controlled Oscillator (VCO) is replaced with the Digital Controlled Oscillator (DCO) [7-11]. The oscillator circuit that employs a digital-intensive approach to regulate the frequency range is commonly referred to as a digitally controlled oscillator (DCO).

The DCOs were invented in the 1980s by the manufactures to overcome the disadvantages of analog controlled oscillators like VCO, PLL etc. A digitally controlled oscillator (DCO) is a type of oscillator circuit which generate an analog type signal; however, its frequency is controlled with the help of input which is digital in nature. According to the today's scenario, most designs are implemented in the CMOS technology. The digital intensive approach improves the circuit designs in terms of flexibility, size, reliability, power consumption, frequency and cost etc. These digitally controlled oscillators are more robust and usually more flexible than the convectional VCOs. In the deep Sub-Micron CMOS technology, the recent trend is implementing digitally controlled RF circuits due to its high integral ability and enhanced

frequency characteristics. There are many technologies exists for the design of DCO circuits like LC topology and ring topology. In oscillator circuits based on ring topology, challenges concerning power consumption can be effectively mitigated through various methodologies, such as enhancing the tuning mechanism of frequency, improving delay stage design, and implementing voltage scaling techniques. In certain applications, electronic systems require a fixed frequency range instead of a variable range of frequencies. For these specific scenarios, Digital Controlled Oscillator (DCO) circuits offer the advantage of generating a fixed range of frequencies with reduced power consumption [10, 12]. To achieve frequency tuning at the output terminal without impacting the overall power consumption, MOS varactors are employed [13].

2. Literature Survey

The utilization of a ring-type oscillator topology offers an enhanced capability to generate a quadrature output without requiring an additional circuit, in contrast to LC oscillators. The frequency of the ring oscillator is inversely proportional to the product of the number of delay stages and the duration of each delay, as represented by Equation (1) [5, 15].

$$F = 1/2Nt_d \quad (1)$$

In Equation (1), 'N' represents the number of delay elements, and 't_d' denotes the propagation delay duration of each individual delay element employed within the ring oscillator.

This HDCRO (Hybrid-Digitally Controlled Ring Oscillator) is configured using three delay cells XNOR gate, CMOS and Pseudo NMOS inverter, where the output frequency of each cell is regulated through digital control bits applied to the MOS varactors. These MOS varactors are utilized to adjust the frequency at the output terminal. In present-day scenarios, MOS varactors are gaining widespread popularity owing to their extensive frequency tuning range and superior quality factor Q in comparison to reverse-biased PN junction diodes. Several methods for implementing MOS varactors have been extensively discussed in the literature [16-18]. These three delay cells are consisting of an inverter implemented with XNOR gate, CMOS and pseudo-NMOS inverter, all of which are controlled with MOS varactors.

A CMOS Pseudo NMOS inverter are different in way of connection of their components as illustrated in fig.1. Both CMOS and Pseudo NMOS inverters consist of one PMOS and one NMOS transistor. However, they differ in their configuration. In the CMOS inverter, the gate of both the PMOS and NMOS transistors is connected to the input terminal. On the other hand, in the Pseudo NMOS inverter, the gate of the PMOS transistor is connected to the ground level, which keeps the PMOS transistor in the 'ON' state, while the gate of the NMOS transistor is connected to the input port.

Pseudo NMOS logic offers several advantages over CMOS inverters. It exhibits superior performance in terms of speed, power consumption, and area utilization compared to CMOS inverter logic.

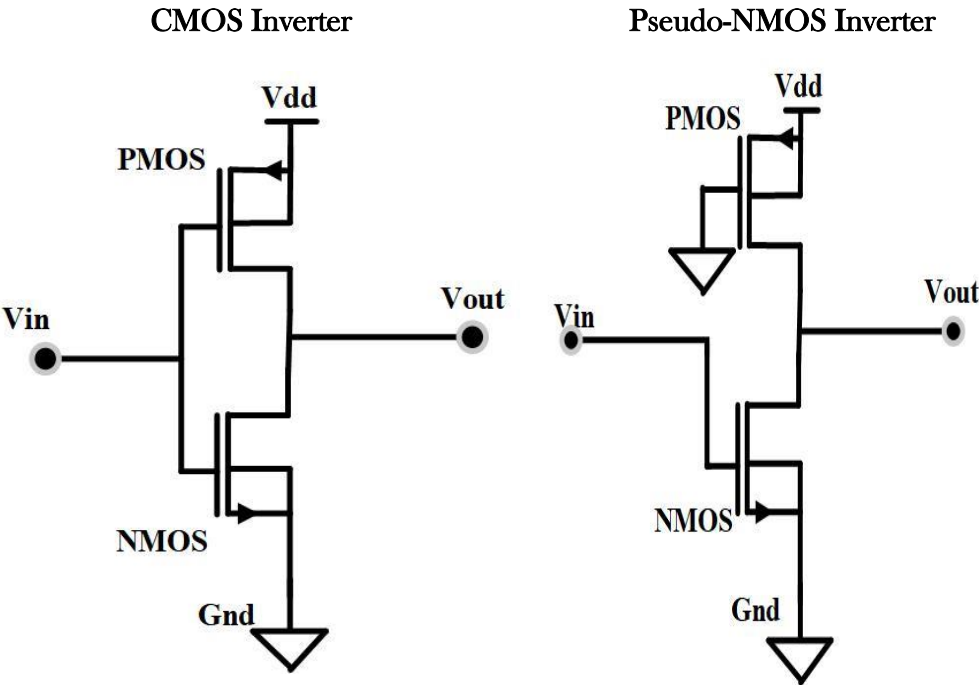


Figure 1. CMOS inverter VS Pseudo-NMOS inverter

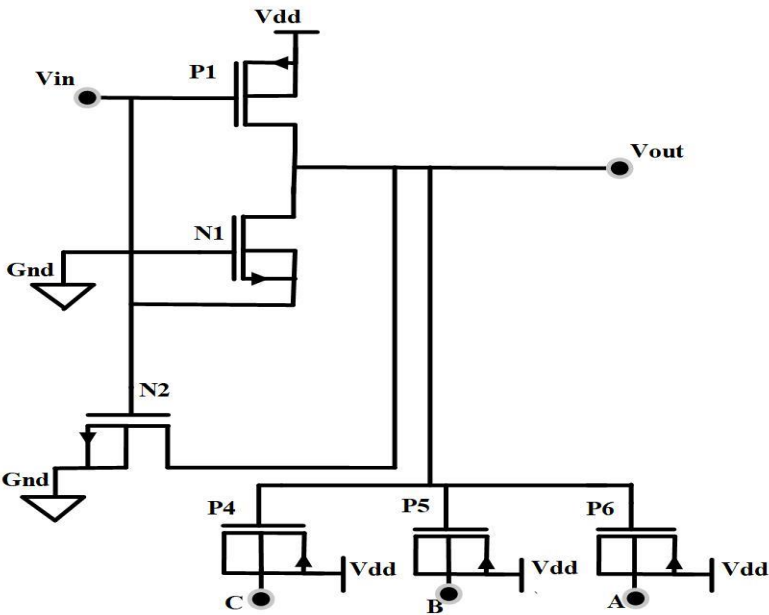


Figure 2. First delay stage of HDCRO circuit

Furthermore, our DCO design incorporates three delay cells. The first delay cell is composed of an inverter implemented with an XNOR gate, comprising three transistors: one PMOS (P1) and two NMOS (N1, N2) transistors. To achieve frequency regulation at the output port, we utilize MOS varactors (P4, P5, P6). The frequency of each cell is precisely controlled by applying specific digital bits (000-111) to the MOS varactor, as illustrated in Figure 2. The second delay cell employs a CMOS-based inverter, consisting of one PMOS (P2) transistor and one NMOS (N3) transistor as shown in figure 2. MOS varactors are used in the same manner as defined above for control the output frequency.

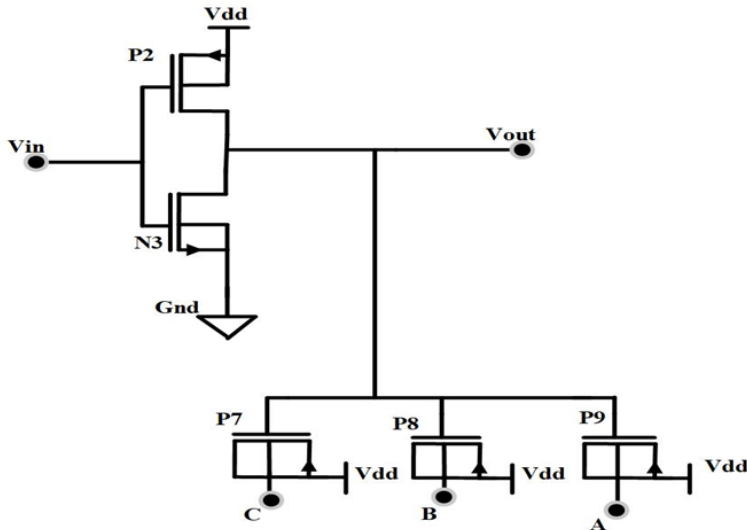


Figure 3. Second delay stage of HDCRO circuit

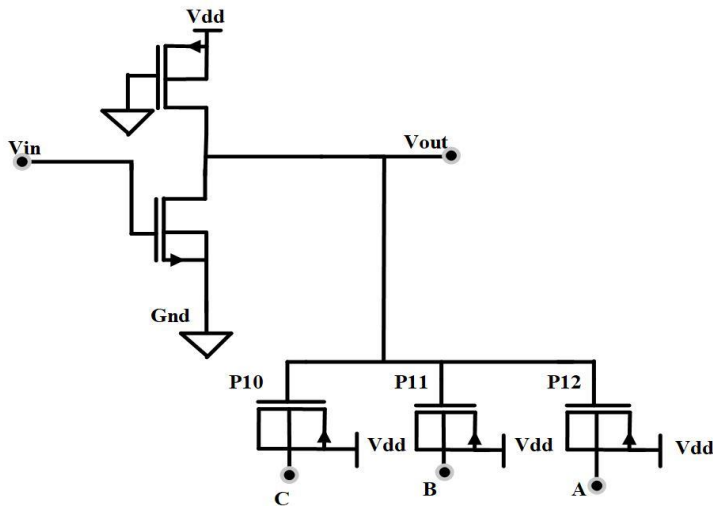


Figure 4. Third delay stage of HDCRO circuit

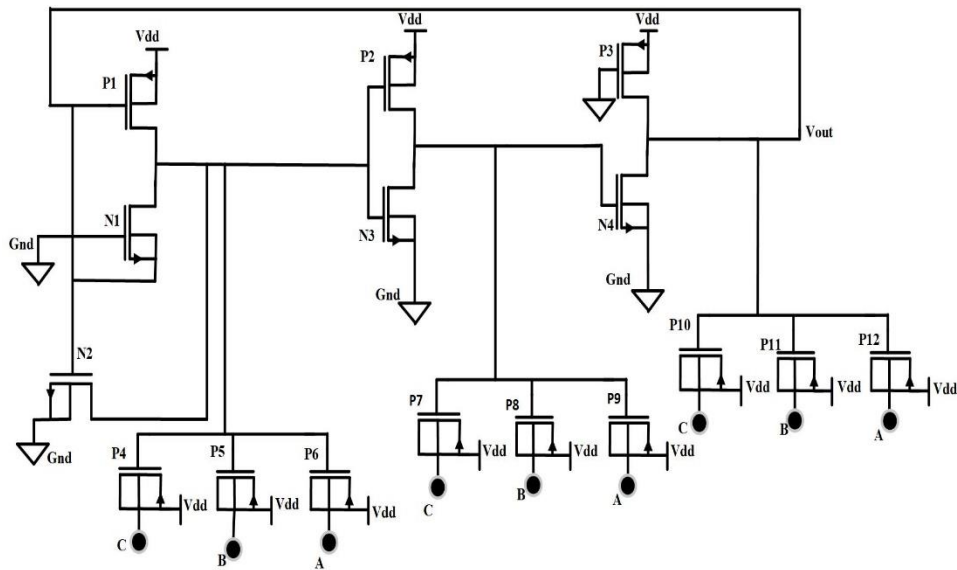


Figure 5. A 3-stage ring HDCRO

Table 1. Width and length specifications of the transistors

Transistors	Width	Length
P1, P2, P3	120nm	100nm
N1, N2, N3, N4	120nm	100nm
P4, P7, P10	120nm	100nm
P5, P8, P11	240nm	100nm
P6, P9, P12	480nm	100nm

The complete 3-stage ring HDCRO circuit which consists of combination of all three delay stages shown in the figure 5. In the 3-stage HDCRO circuit designing the specifications of width and length is taken as defined in the Table-1, we can set the value of width according to need while the value of length is by default taken 100nm in the 90nm technology model file defined in cadence tool. Figure 5 represents the proposed Hybrid Digitally Controlled Ring Oscillator (HDCRO) by employing the above discussed delay stages organized in a ring configuration, as depicted in. The DCO circuit consists of three stages, and the output signal from one stage serves as the input for the next stage. The output signal derived from the final delay configuration is connected back to the initial point, forming a closed circuit. To achieve precise regulation of the DCRO frequency, digital bits C, B, and A are manipulated [18-22].

3. Simulation Results

Table 2. Variation of HDCRO Frequency with MOS varactor control bits

Control bits C B A	Power consumption (mW)	Frequency (in GHz)	Phase noise (dBc/Hz)
0 0 0	3.638	2.558	-68.070 @1MHz
0 0 1	2.604	2.571	-68.004 @1MHz
0 1 0	2.602	2.587	-67.934 @1MHz
0 1 1	1.568	2.601	-67.866 @1MHz
1 0 0	2.081	2.618	-67.797
1 0 1	1.047	2.633	-67.725
1 1 0	1.046	2.649	-67.654

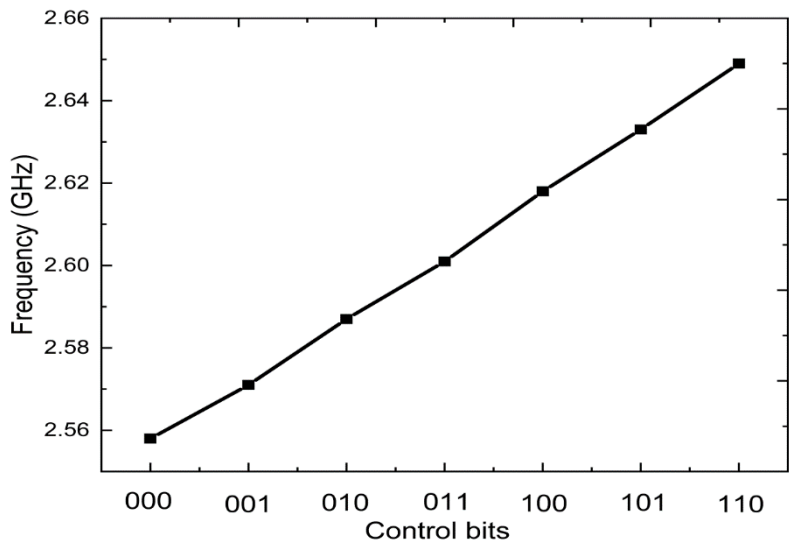


Figure 6. Variation of Frequency with Digital control bits

The HDCRO circuit proposed in this study is designed using TSMC 90 nm CMOS technology. The design's performance has been thoroughly assessed through extensive simulations utilizing the Cadence simulation tool. The closed ring structure allows for achieving a variable frequency by carefully controlling the delay duration of each delay element.

Table 2 presents a comprehensive analysis of the impact of three digital control bits provided to MOS varactors, on the power consumption and output frequency within the presented HDCRO system. The operating voltage is selected to be 0.7 V. The concurrent manipulation of these control bits influences the capacitance of each delay element, resulting in

frequency variations within the **HDCRO** circuit. Based on the combination of the control bits the load capacitance of varactor diode varies, which results in variation in the frequency of generated signal. It can be seen in table with the increase in binary bits, the frequency of the signal increases thus following a linear relation.

Through complete examination of all possible combinations of digital control bits, it is observed that the **HDCRO** operates effectively within a frequency range spanning from 2.558 GHz to 2.649 GHz. Table 2 provides a comprehensive depiction of the frequency variations that occur as a direct consequence of the digital control bits of MOS varactors, exhibiting a frequency range of 2.558 GHz to 2.649 GHz, along with corresponding power fluctuations ranging from 3.638 mW to 1.046 mW for bits 000 to 110 (C B A).

Additionally, Table 3 showcases the frequency changes resulting from voltage variations ranging from 0.6 V to 1 V. The recorded frequencies in this case span from 1.238 GHz to 4.438 GHz, accompanied by power deviations spanning from 28.86 μ W to 54.66 mW for bit 110 (C B A). These findings offer valuable insights into the frequency and power dynamics of the **HDCRO**, based on various digital control bit configurations and voltage levels.

Among the various parameters, the noise characteristics of the oscillator circuit are of particular significance as they significantly impact the quality of the generated carrier signals. The impact of the variation of three control bits on the phase noise parameter is presented in Tables 2 and 3.

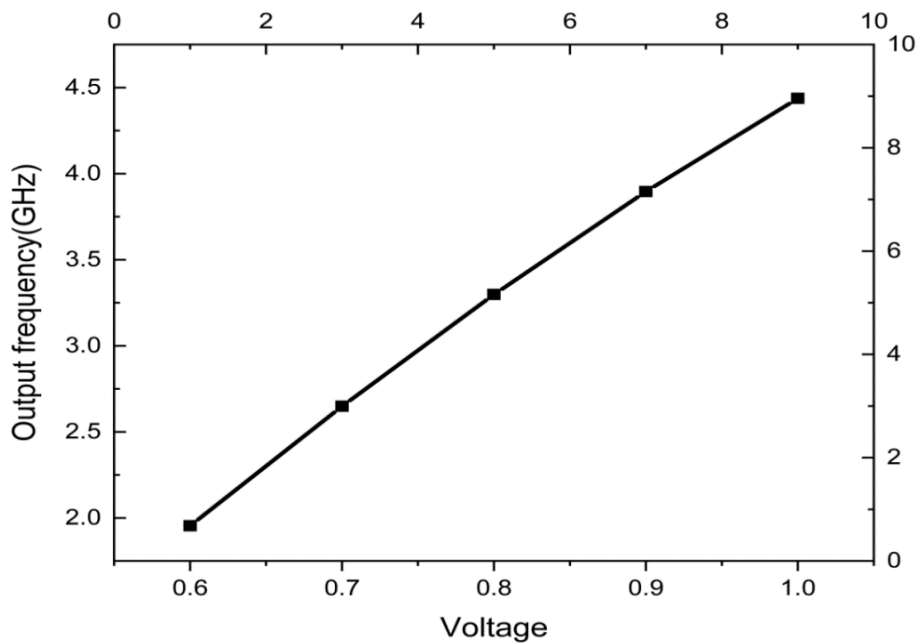


Figure 7. Variation of Frequency with Voltage

Table 3. Variation of Frequency with supply voltage (Vdd)

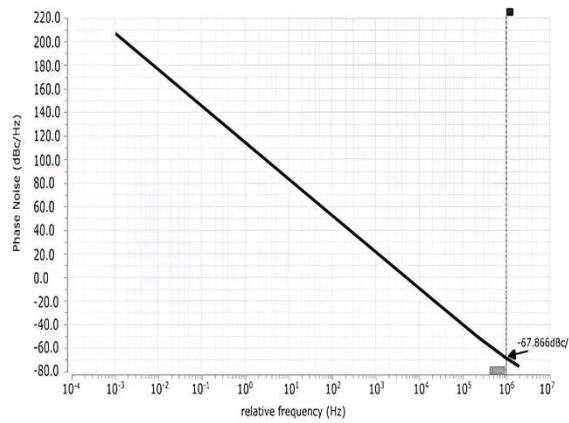
Voltage supply (Vdd)	Power consumption	Frequency (in GHz)	Phase noise (dBc/Hz)
0.6V	28.86μW	1.955GHz	-68.390dBc/Hz
0.7V	1.046mW	2.649GHz	-67.654dBc/Hz
0.8V	10.28mW	3.298GHz	-66.821dBc/Hz
0.9V	29.17mW	3.896GHz	-66.083dBc/Hz
1.0V	54.66Mw	4.438GHz	-65.445dBc/Hz



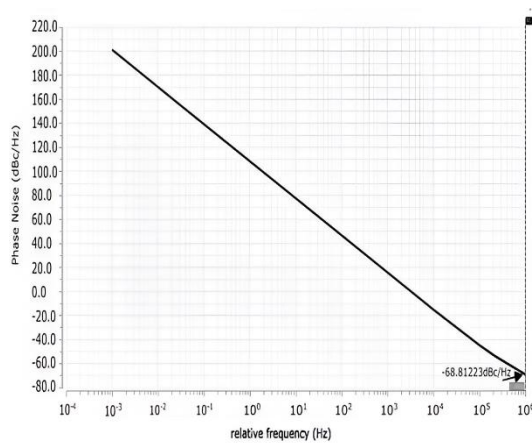
Figure 8. Output waveform of 3-stage ring HDCRO

Table 4. Performance comparison of proposed circuit design with the existing literature

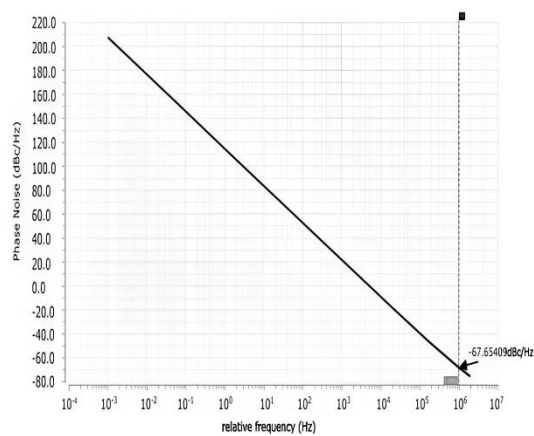
Ref.	Technology (nm)	Voltage (V)	Power (mw)	Frequency (GHz)	Phase noise (dBc/Hz)
[9]	180	1.8	4.397	0.89-0.916	-93.905@1MHz
[15]	180	1.8	1.624	0.818-0.872	-101.24@1MHz
[16]	90	1.2	4.9	10	-116@1MHz
[17]	90	2.3	2.3	52.3	-116.5@1MHz
[18]	90	14	14	58.7	-114@1MHz
Proposed work	90	0.7	1.046	2.55-2.64	-67.654@1MHz



(a)



(b)



(c)

Figure 9. Results of HDCRO Phase noise (a) 011 at 0.7V (b) 110 at 0.7V (c) 110 at 0.5V

4. Conclusion

This paper presents a new delay stage based three-bit hybrid-digitally controlled ring oscillator (HDCRO) implemented in TSMC 90nm CMOS technology. The proposed new HDCRO circuit gives low-power consumption as compared to the other literate circuits. The power consumption of each delay cell is efficiently regulated by implementing MOS varactor-based load capacitance. The frequency variation occurs as a result of changing the digital control bits of the MOS varactors at a supply voltage of 0.7 V, consequently modifying the load capacitance. The proposed HDCRO demonstrates an oscillation frequency range of 2.558 GHz to 2.649 GHz, with power consumption varying from 3.638 mW to 1.046 mW, and phase noise ranging from -68.070 dB@1 MHz to -67.654 dB@1 MHz relative to the central oscillation frequency. Moreover, by applying a supply voltage variation between 0.5 V and 1 V, a wider frequency tuning range of 1.238 GHz to 4.438 GHz is achieved. This extended tuning range exhibits power consumption variation from 2.785 μ W to 54.66 mW, and phase noise ranging from -68.812 dB@1 MHz to -65.445 dB@1 MHz relative to the central oscillation frequency.

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Conflict of interest

The Author's have no conflicts of interest to declare that they are relevant to the content of this article.

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