RESEARCH ARTICLE

DOI: 10.34256/famr2512

Frontiers in Advanced Materials Research

Energy-Saving Triggering Series Low-Power, High-Performance Locking Systems for Element Design

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Received: 17-12-2024, Revised: 12-04-2025, Accepted: 28-04-2025, Published: 03-05-2025

Abstract: Flip-flops represent a significant source of power dissipation within a system. The clocking system itself comprises sequential components, such as latches and flip-flops, alongside the network that delivers clock signals. The pseudo-NMOS technology, split path, and clock tree sharing schemes are employed to propose a positive edge triggering flip-flop that is designed for both speed and power efficiency. The flip-flop's latching section's floating node instability and inadequate circuit energy loss are solved via pseudo NMOS and split path approaches, respectively. By enabling the latching part of the flip-flop to share the clock provision network for gathering the data D, the clock tree sharing technique reduces the D-Q delay and the overall number of transistors required to construct the clock provision network. Cutting back on the number of clocked loads is one method that reduces dynamic power dissipation and switching activity. The flip-flop's latching part is made using this process in the suggested design. This study evaluates the performance of a flip-flop circuit modeled using 0.12 nm CMOS process technology. According to the simulation comparison, the suggested register element design improves The power delay product increased from 56.86th% to 71.26th%, the energy delay product rose from 77.86th% to 82.4th%, and the power energy product (PEP) escalated from 56.22th% to 81.22th%. It conserves between 7.06th% and 32.83rd% of energy.

Keywords: Low Power, Sequential Element (flip-flop), Digital CMOS, Single Edge Triggering.

1. Introduction

Power consumption was previously seen as a secondary concern in the design of VLSI circuits, with space, performance, and cost being the main considerations. Energy consumption is now regarded being among the main issues in Modeling of VLSI Circuits, reversing this tendency. One explanation is that power consumption has become a key consideration in VLSI

circuit design due to the steadily increasing operating frequency and the development in chip scale of integration. In addition to discouraging their usage in portable devices, integrated circuits' significant power dissipation leads to overheating, which reduces system longevity and performance. Power dissipation directly affects the chip's packing and the system's coding costs. The designers of VLSI systems are motivated by all of these considerations to minimize circuit power dissipation and to view it as a significant problem one of the main parts of the VLSI system that uses the most power is the clocking system [1, 2]. It makes up between 30 and 60 percent of the system's overall power dissipation [3]. The power consumption of a certain clocking mechanism can be expressed as [4, 5].

$$P_{clk-system} = P_{clk-Pnw} + P_{seq-elements[ff]} \quad (1)$$

Where Pclk-Pnw and Pseq-elements represent the power consumption of the clock provision network and the sequential elements (flip-flops), respectively. The clock allocation tree's power consumption can be expressed as follows:

$$P_{clk-pnw} = \{(C_{int\_line} + C_{clk\_load})V^2{}_{clk-swing}\} * f_{clk} \quad (2)$$

Where V2clk-swing represents the clock swing voltage, fclk stands for the clock frequency, Cint_line for the interconnect line capacitance, and Cclk-load for the capacitance of the clocked transistor loads of the respective sequential components.

The following is an expression for the power used by the successive elements:

$$P_{seq-element} = \{(\alpha_i c_i \beta + \alpha_0 c_0 \beta_0 + C_{clk-Buf}) * V^2{}_{dd}\} * f_{clk} \quad (3)$$

In this case, ci is the register element's internal node capacitance, co is its output capacitance, and i and o are the internal and output nodes' switching activity ratios, respectively. In a register, the clocking buffers have an electrical resistance of Cclk-Buf, and fclk is the frequency of the timing. And α is the trigger factor. Flip-flops with single-edge triggering have a value of 1, whereas those with double-edge triggering have a value of 2. Consequently, it is critical to reduce the energy usage of the clock provider network and sequential components (flip-flops). Therefore, lowering the power used by the flip-flops will significantly affect the clocking system's overall power usage. [6].

Programmable pulse-triggered and master-slave flip-flops are used in many digital applications and microprocessors nowadays. A pair of latches, one transparent high and the other transparent low, are used to create a conventional master-slave flip-flop [7]. Both single-edge and double-edge triggers are possible. They are distinguished by hard edge characteristics including a significant D to Q delay caused by a positive setup time. The SAFF flip-flop, which is based on a sense amplifier, is another edge-triggered flip-flop [8]. A short D-to-Q delay is the consequence of a negative setup time in pulse-triggered flip-flops, which are two-stage combined devices with a soft edge feature.They could be divided into two categories. Both explicit and implicit pulse-

triggered flip-flops have been developed [9, 10]. A digital CMOS circuit may dissipate power from three different sources. Power dissipation can be either static, dynamic, or short circuit. The clocking system's overall power dissipation can be written as.

$$P_{total} = P_{static} + P_{dynamic} + P_{short} \quad (4)$$

Pstatic power dissipation results from ongoing current drain from the power availability, including leakage current. Pdynamic, or dynamic power dissipation, is brought on by transient current switching as well as load capacitance charging and discharging. Short circuit power dissipation, or Pshort, occurs when the n-sub and p-sub networks of a complementary metal-oxide semiconductor gate (CMOS) gate conduct at the same time.

The following list of different approaches of lowering power consumption is based on these factors:

1) Reducing the clocked load's capacity
2) lowering swing clocking
3) Reducing the severity of punishments
4) Minimizing the duration of power outages
5) Minimizing leaks and static electricity, as well as capacitance
6) Applying the principle of split routes

2. Pseudo-NMOS LOGIC

For circuit design, the majority of the n-type Field Effect Transistors (nFET) used in the NMOS logic family. NMOS was the dominating technology before CMOS, but it is already outdated. The circuits of pseudo-NMOS logic, a CMOS technology, resemble those of the earlier nFET-only NMOS logic family networks [11]. In Figure 1, a basic NMOS inverter is displayed. One NMOS transistor functions as a driver to regulate the inverter circuit. As a pull-up device, the load resistor RL is connected to the power supply VDD. It consistently raises the output voltage to VDD. As seen in Figures 2 and 3, the load transistor RL in pseudo-NMOS logic is swapped out for an always biased-ON PMOS transistor. The NMOS logic array is the only tool used to create logic, and it pulls the circuit down to ground VSS. Logic arrays do not contain PMOS transistors. The interconnect wiring is made simpler. This is the main benefit of this reasoning.

The main advantage of this logic is that, unlike static CMOS logic, which employs 2N transistors, it only uses N+1 transistors. [12]. the floating node issue between the logic circuit's input and output nodes is effectively avoided by this logic. In this logic, the high output voltage is VDD, and the low output voltage is not zero volts for each gate. A comparable reduction in the interference margin occurs. The primary challenge with this logic is staticpower of dissipation, which occurs whenever the pull-down NMOS logic network is turned on.

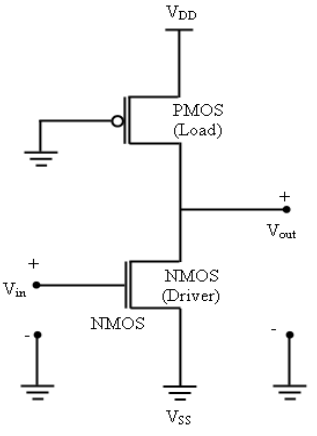

Figure 1. Logic inverter utilizing pseudo-NMOS

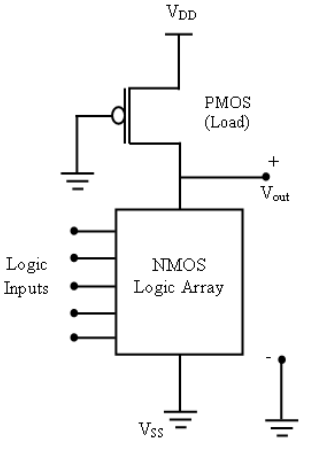

Figure 2. Integrating pseudo-NMOS logic into an NMOS logic array

Since the PMOS transistor is regularly on, a direct current flow occurs between VDD and VSS ground while the NMOS pull-down network has been turned on. In circuit design, ratioed transistors are used as much as possible to reduce static power usage and maintain a low output voltage. To guarantee the appropriate noise margin for this logic, the transistors must be scaled appropriately [13].

3. PN-SETFF Register Element Proposed

Here we present the PN-SETFF, a positive edge-triggering flip-flop that is based on pseudo NMOS technology. Only at the clock signal's positive edge (CLK=1) does it record the incoming data. It requires a total of 12 transistors and is divided into two sections: the latching part and the clock allocation section. As seen in Figure 3, this flip-flop requires four timed transistors out of a total of twelve transistors.

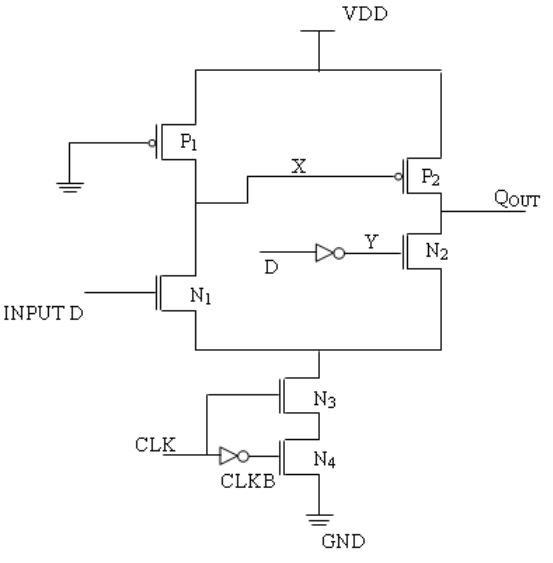

Figure 3. Positive Edge Triggering Flip-Flop based on Pseudo NMOS (PN-SETFF)

The suggested flip-flop has a lower number of clocked loads. In this architecture, the switching activity is decreased by lowering the amount of timed loads. Because clocked transistors have far more switching activity than transistors that are not clocked.

There are two phases in the latching section. Transistors P1 and N1 build the first stage, whereas P2 and N2 build the second. This design uses pseudo NMOS technology at the latching section's initial stage. Because of its permanently grounded gate, the always on is the P1 transistor in the first stage. [14].

A constant-on pseudo NMOS transistor P1 charges the internal node X, situated between the first and second stages, to the supply voltage VDD. Therefore, node X will never be a floating node and will always remain connected between the latching stages. This PN-SETFF design avoids the floating node issue.

Another power-saving method used in this flip-flop design is the split path approach. The second latching stage's outside discharge path contains the NMOS transistor N2. Only the PMOS transistor P2 is driven by an intermediate node X; the N2 discharge transistor is not driven by it. The input data D asserts an inverter I1, at node Y, the signal is transmitted. Node Y can only drive one NMOS transistor, the discharge NMOS transistor N2. As a result, two distinct signals from nodes X and Y, respectively, drive transistors P2 and N2 in the second latching stage Because of this, the dissipation of power in a short circuit is reduced, and the possibility of shorting out transistors P2 and N2 is eliminated.

The two NMOS transistors N3 and N4 in this configuration form the clock allocation network. This design also uses a clock allocation network sharing technique. P1, N1, and P2, N2

are two latching stages that share the clock allocation network for sampling the input data D. Not only does this sharing strategy drastically cut down on D-Q latency, but it also reduces the power consumption and transistor count of the clock allocation network.

This suggested element works as follows: CLK rises when D=HIGH, and CLKB remains high for a brief period of time, equivalent to one inverter delay. N3 and N4, two clocked branch NMOS transistors, will go into active-state during this period as the flip-flop enters its evaluation phase. The initial stage of the latching component is in charge of loading the transition from 0 to 1 data input. When the internal node X discharges, the output Q=1.

As CLK goes down, CLKB goes up, and the D input stays HIGH. Node X is unable to participate in redundant switching since the first stage is disconnected from the ground in these conditions. The second step is in charge of recording the data transitions from 1 to 0. When the second stage's pull-down network is turned on during this transition, output Q=0 results.

Clock sharing, split path techniques, and the pseudo NMOS technology all lower total power consumption and increase PN speed.-SETFF.

4. Overviews and Discusses

The results of the simulations were obtained using room temperature 0.12 nm CMOS fabrication technology and DSCH and Microwind simulations. Every possible circuit design is mimicked at the layout level. In modern digital CMOS logic design, an activity factor of about 0.1 is common for a clock with an activity factor of about 1. Transistors that are directly driven by the clock in both the logic branch and the clock pulse generator are regarded as 100% switching activity transistors in this architecture.

A constant clock frequency of 125 MHz is maintained. The circuit is alternately supplied with the input data D (0, 1), and its functionality is confirmed. The circuits' power consumption is evaluated. Data to output (D to Q delay) is the unit of measurement for delay.

The power delay product (PDP) is a standard statistic for optimizing electronic design that reduces both power consumption and design latency. Both power and delay are given neutral geometric weights. When

Assessing the design's quality, EDP is a helpful metric to employ [15]. Energy Delay Product (EDP) is the formula for it. When performance is of utmost importance, this metric is suitable.

If power is more important, then it's possible that neither the EDP matrix nor the PDP matrix will yield better results. Here, we take a look at the power energy product (PEP), a new metric [16, 17]. It yields a lower power solution than the other two matrices and provides more geometric weight to power than delay. The formula for PEP is Power divided by Energy.

Both the positive and negative edges of the clock arrivals are used to sample data in SETFF. We test the suggested PN-SETFF circuit in four different scenarios, and it works by sampling the input data D on the positive edge of the clock signal.

First operation:

Input- data D=0, CLK, =1, CLKB=0; output -Q=0& Qb= 0

Second operation:

Input- data D=1, CLK, =0, CLKB=1; output- Q=0 & Qb= 1

Third operation:

Input- data D=0, CLK, =1, CLKB=0; output -Q=1& Qb= 0

Fourth Operation:

Input- data D=0, CLK, =0, CLKB=1; output -Q=0 & Qb= 0

Figure 4. reveals the circuit illustration for the suggested flip-flop design in the DSCH tool. The aforementioned functioning of the suggested circuit is demonstrated in Figures 5, 6, 7, and 8, respectively, under various sets of input D and CLK signals. Figure 9 displays the proposed PN-SETFF's output waveform with power consumption, while Figure 10 depicts its physical configuration. [18, 19].

The significance and potential of the suggested flip flop design are assessed in compari son to the current designs using performance metrics like total number of transistors, number o f clocked transistors, layout area (A), power consumption (P), delay (DQ), and optimization me trics like power of delay product , Energy of delay product , and power energy product.

To assess the importance and potential of the suggested flip flop design in comparison to the current designs, performance metrics like total number of transistors, number of clocked transistors, layout area (A), power consumption (P), delay (D-Q), and optimization metrics like power delay product (PDP), energy delay product (EDP), and power energy product (PEP) are used. [20]

In terms of performance characteristics and optimization metrics, Tables 1 and 2 show the results of the current sequential elements (flip-flops), whereas Tables 3 and 4 show the results of the proposed PN-SETFF design. Performance metrics like total transistor count and number of clocked loads are presented in bar charts for easy comparison. Figure 11, Figure 12 for layout area, Figure 13 for power consumption, Figure 14 for delay, and other information for optimization metrics like PDP, EDP, and PEP are displayed [21]. As seen in Figure 15, Table 1 & 2, 3, 4 shows the outcomes of the suggested PN-SETFF design and the current sequential elements (flip-flops) in terms of optimization metrics and performance parameters, respectively.

Table 1. Performance Criteria A comparison between the suggested and current sequential elements

Sequential Elements	Performance parameters					
	Total Transistors (TT)	Clocked Transistors (CT)	Triggering Mode (TM)	Area (μm^2)	D -Q Delay (ps)	Total Power (µw)
SPGFF	30.0 Nos	16.0 Nos	Double	546val	162val	16.4val
POWER PC	22.0 Nos	8.0 Nos	Single	429val	176	13.424
HLFF	20.0 Nos	10.0 Nos	Single	312val	158	12.276
XCFF	21.0 Nos	4.0 Nos	Single	338val	163	11.123
SDFF	23.0 Nos	7.0 Nos	Single	264val	156	11.028
CDMFF	22.0 Nos	7.0 Nos	Single	429val	178	10.277
DDFF	18.0 Nos	6.0 Nos	Single	299val	166val	9.725val
CTS-DETFF	23.0 Nos	8.0 Nos	Double	424val	179	8.347
Proposed Sequential Element PN - SETFF	11.0 Nos	4.0 Nos	Single	182	65	6.647

Table 2. Efficiency Measures Evaluation of Current Elements with Respect to the Proposed Sequential Elements

sequential Element	Efficiency Measures		
	PDP (fj)	EDP ($\times 10^{-24}$)	PEP ($\times 10^{-30}$)
SPGFF	2.656val	0.430val	4.355val
POWER PC	2.362val	0.415val	3.170val
HLFF	1.939val	0.306val	2.380val
XCFF	1.813val	0.295val	1.135val
SDFF	1.720val	0.26val	1.896val
CDMFF	1.829val	0.325val	1.879val
DDFF	1.614val	0.267val	1.131val
CTS-DETFF	1.503val	0.2690val	1.263val
Proposed sequential Element PN - SETFF	0.398	0.0224	0.282

The performance metrics are displayed in bar charts for easy comparison, including Figure 11 shows the total number of transistors and clocked loads; Figure 12 shows the layout area; Figure 13 shows the power consumption; Figure 14 shows the delay; and Figure 15.

Upon examining the characteristics in Table 1, it can be seen that the suggested PN-SETFF employs a total of 12 transistors, including 4 timed loads. When compared to the current elements, this is the bare minimum of transistors. When compared to conventional sequential elements, PN-SETFF reduces the total number of transistors by 33.33% to 60% and the clocked transistors by 33.33% to 75%, with the exception of XCFF. The four clocked load numbers of the register element XCFF match the clocked load counts of the suggested PN-SETFF.

The floating node issue is successfully resolved by the suggested PN-SETFF design, which employs the pseudo NMOS technology. Through a pseudo NMOS transistor P1 that is always in the ON state, the internal node X, which is located between the first and second stages, is charged to supply voltage VDD. Therefore, node X will never be a floating node and will always remain connected between the latching stages. The floating node issue in the suggested PN-SETFF design is effectively avoided by the pseudo NMOS approach.

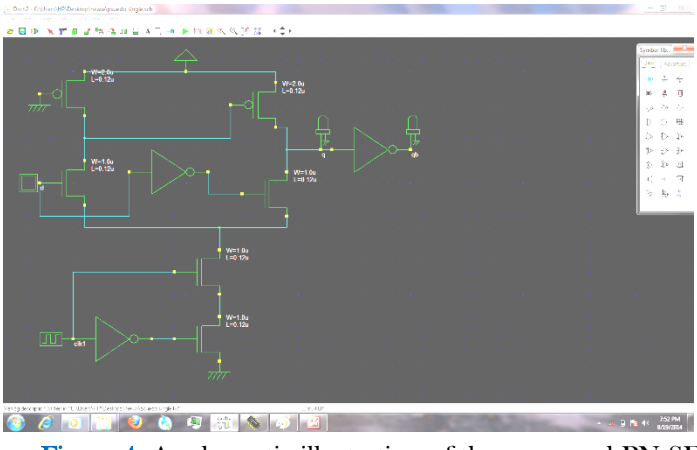

Figure 4. A schematic illustration of the proposed PN-SETFF

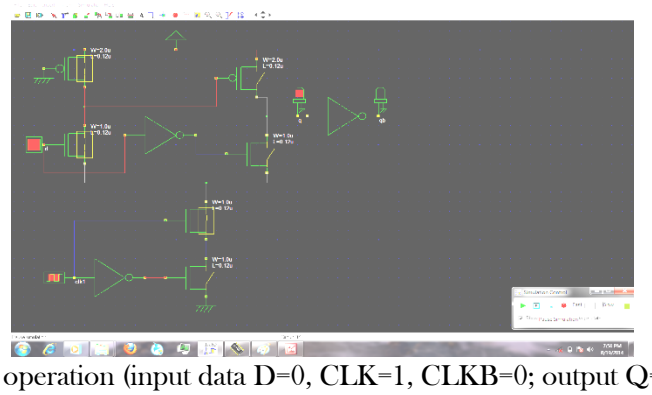

Figure 5. First operation (input data D=0, CLK=1, CLKB=0; output Q= 0& Qb= 0)

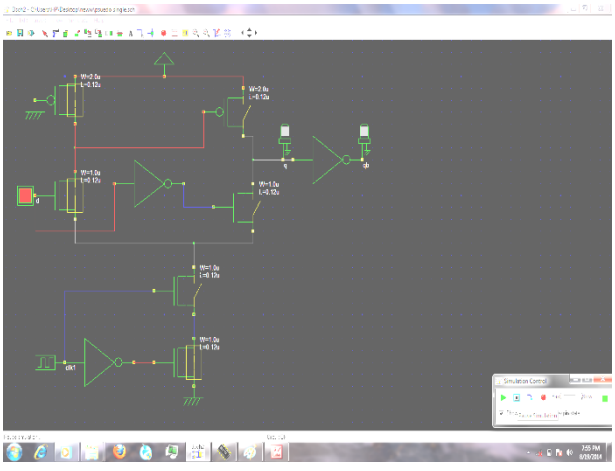

Figure 6. Second Operation: Input data D=1, CLK=0, CLKB=1; output Q=0 & Qb= 1)

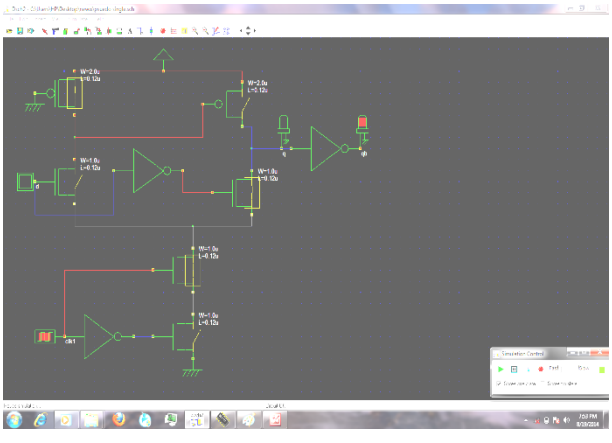

Figure 7. Third Operation: (Input data D=0, CLK=1, CLKB=0; output Q=1 & Qb= 0)

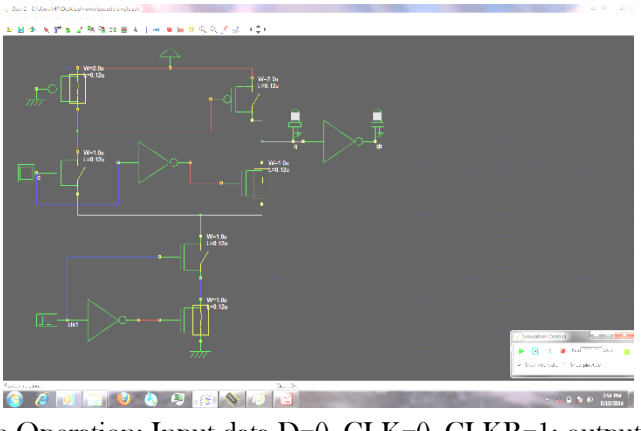

Figure 8. Fourth Operation: Input data D=0, CLK=0, CLKB=1; output Q=0 & Qb= 0)

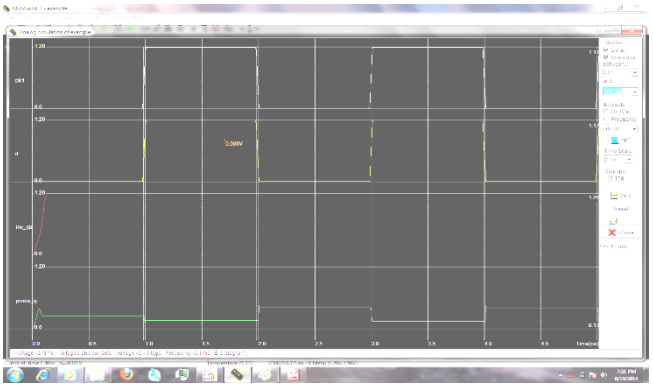

Figure 9. The proposed PN-SETFFs output waveform has a power consumption of 6.674µw.

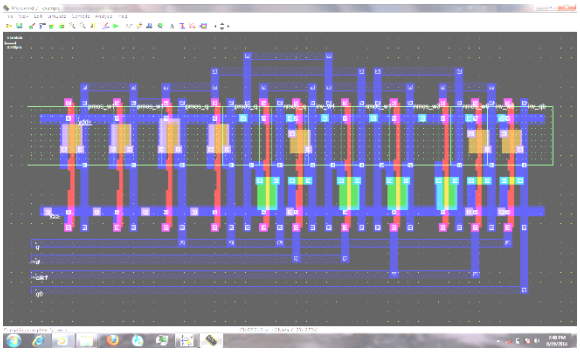

Figure 10. Schematic Plan of the Envisioned PN-SETFF (area= 182µm^2)

The 182µm^2 area is occupied by the suggested PN-SETFF. When compared to current sequential elements, this proposed design uses 31.06% to 66.66% less space.

The planned PN-SETFF has a 65ps delay due to the D-Q delay. When compared to other sequential items, this delay value is significantly lower. Component parts.

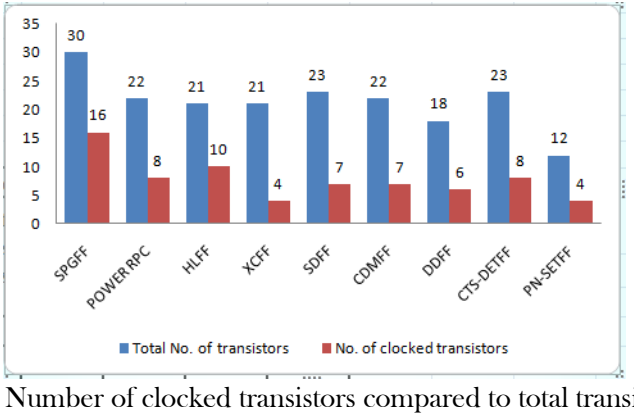

Figure 11. Number of clocked transistors compared to total transistors

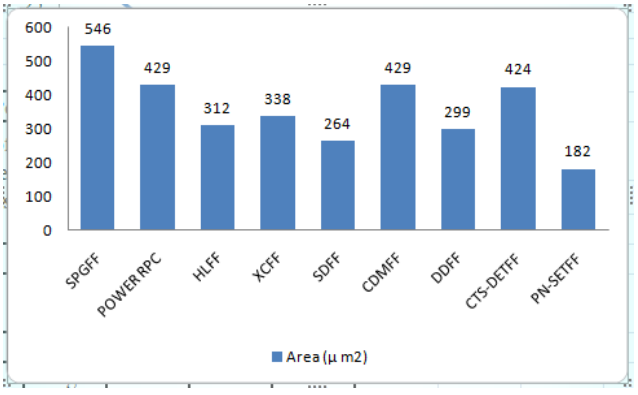

Figure 12. Evaluation of the used space in a given arrangement

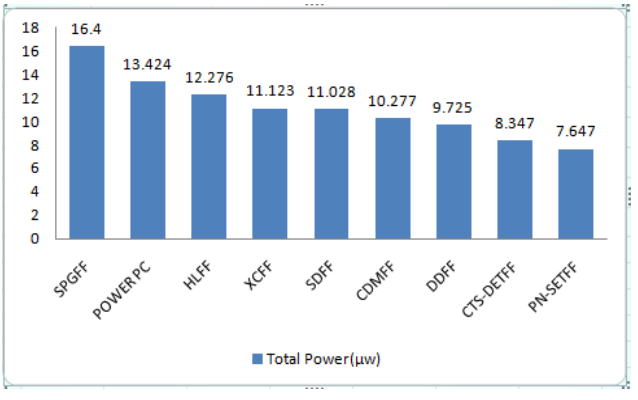

Figure 13. Examining overall power usage trends

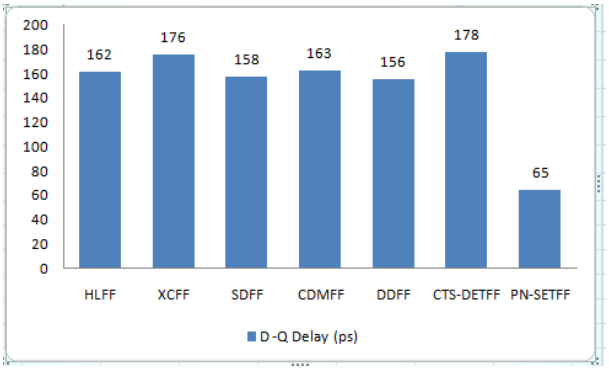

Figure 14. Analyzing the D-Q delay

According to the data, the overall power consumption of the suggested PN-SETFF is 7.674 µw. Compare to all the sequential items that are already present in Table 1. A power reduction of 8.06–42.83% is achieved by this design.

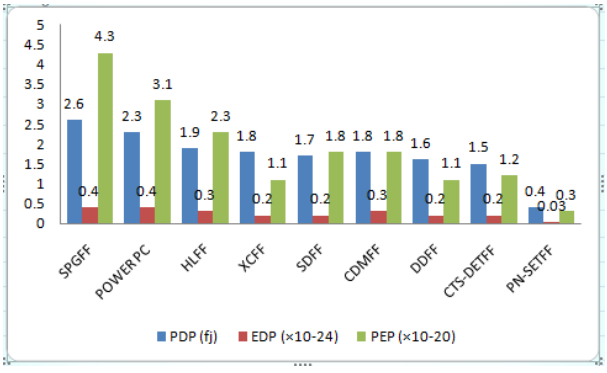

Figure 15. Evaluation of PDP, EDP, and PEP (Power Energy Product) in Relation to One Another

By contrasting Table 2's values, the suggested PN-SETFF has a PDP value of 0.398 fj in the PDP point. When compared to all of the flip-flops in Table 2, it has improved by 66.86% to 81.25%. The suggested PN-SETFF has a value of 0.0224×10-24 in light of EDP. When compared to all current flip-flops and CTS-DETFF, the proposed PN-SETFF's EDP value increased from 87.86% to 92.46%. With a PEP value of 0.282×10-20, the suggested PN-SETFF outperformed the current sequential components by 66.22% to 91.22%.

5. Conclusion

This paper proposes the PN-SETFF, a clocking device based on pseudo NMOS technology that is both low power and high performance. The floating node issue is successfully resolved by the pseudo NMOS approach used in the design of this suggested piece. It uses the split path approach, which lowers the power dissipation from short circuits. The number of clocked transistors in this architecture is reduced to four by employing the method of reducing the number of clocked loads. The switching activity of clocked transistors is significantly higher than that of unclocked transistors. By reducing the number of timed loads, this proposed design minimizes switching activity and hence reduces dynamic power dissipation. This design also uses a clock providing network sharing method. The input data D is collected by the first and second latching stages of this flip-flop architecture over the shared clock allocation network. The power consumption of the clock provision network is greatly decreased by this sharing technique, which also successfully lowers the number of transistors needed to build the clock allocation network.

Overall, the suggested PN-SETFF's power consumption is reduced by 6.674µw and its delay value is lowered by 65 ps thanks to the pseudo NMOS technology, split path, fewer clocked loads, and clock provision network sharing strategies. The suggested element's optimization metrics have been adjusted to PDP = 0.398 fj, EDP = 0.0224×10-24, and PEP = 0.282 ×10-20. The suggested sequential element may be appropriate for low power and high performance clocking systems because of its significant D-Q delay and low power consumption.

References

[1] Zhao, P., McNeely, J., Kuang, W., Wang, N., Wang, Z. (2010). Design of sequential elements for low power clocking system. IEEE Transactions on very large scale integration (VLSI) systems, 19 (2011), 914 – 918. https://doi.org/10.1109/TFUZZ.2011.2150757

[2] Kawaguchi, H., & Sakurai, T. (2002). A reduced clock-swing flip-flop (RCSFF) for 63% power reduction. IEEE journal of solid-state circuits, 33(5), 807-811. https://doi.org/10.1109/4.668997

[3] Johnson, T.A., Kourtev, I.S. (2011) a single Latch, high-speed double-edge triggered flip-flop (DETFF), in proc. IEEE International Conference on Electronics, Circuits and Systems, 189-192. https://doi.org/10.1109/ICECS.2001.957712

[4] Kim, C., Kang, S.M., (2002), A low-swing clock double edge-triggered flip-flop, IEEE J. Solid-State Circuits, 37, 648-652. https://doi.org/10.1109/4.997859

[5] Gerosa, G., Gary, S., Dietz, C., Pham, D., Hoover, K., Alvarez, J., Sanchez, H., Ippolito, P., Ngo, T., Litch, S. and Eno, J., 1994. A 2.2 w, 80 mhz superscalar risc microprocessor. IEEE Journal of Solid-State Circuits, 29(12), 1440-1454. https://doi.org/10.1109/4.340417

[6] Yuan, J., Svensson, C. (2002). High-speed CMOS circuit technique. IEEE journal of solid-state circuits, 24(1), 62-70. https://doi.org/10.1109/4.16303

[7] Nikolic, B., Oklobdzija, V. G., Stojanovic, V., Jia, W., Chiu, J. K. S., & Leung, M. M. T. (2000). Improved sense-amplifier-based flip-flop: Design and measurements. IEEE Journal of Solid-State Circuits, 35(6), 876-884. https://doi.org/10.1109/4.845191

[8] Strollo, A. G., De Caro, D., Napoli, E., & Petra, N. (2005). A novel high-speed sense-amplifier-based flip-flop. IEEE transactions on very large scale integration (VLSI) systems, 13(11), 1266-1274. https://doi.org/10.1109/TVLSI.2005.859586

[9] Partovi, H., Burd, R., Salim, U., Weber, F., DiGregorio, L., & Draper, D. (1996, February). Flow-through latch and edge-triggered flip-flop hybrid elements. In 1996 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC, and IEEE. 138-139. https://doi.org/10.1109/ISSCC.1996.488543

[10] Hwang, Y.T., Lin, J.F., Sheu, M.H. (2011). Low-power pulse-triggered flip-flop design with conditional pulse-enhancement scheme. IEEE transactions on very large scale integration systems, 20(2), 361-366. https://doi.org/10.1109/TVLSI.2010.2096483

[11] Nedovic, N., Oklobdzija, V.G. (2005). Dual-edge triggered storage elements and clocking strategy for low-power systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 13(5), 577-590. https://doi.org/10.1109/TVLSI.2005.844302

[12] Hirata, A., Nakanishi, K., Nozoe, M., Miyoshi, A. (2005) The cross charge-control flip-flop: A low-power and high-speed flip-flop suitable for mobile application SoCs', In Digest of Technical Papers. 2005 Symposium on VLSI Circuits, 306–307. https://doi.org/10.1109/VLSIC.2005.1469392

[13] Klass, F., Amir, C., Das, A., Aingaran, K., Truong, C., Wang, R., Mehta, A., Heald, R. and Yee, G.(1999) A New Family of Semi dynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors. IEEE Journal of Solid-State Circuits, 34(5), 712-716. https://doi.org/10.1109/4.760383

[14] Teh, C.K., Hamada, M., Fujita, T., Hara, H., Ikumi, N., Oowaki, Y. (2007). Conditional data mapping flip-flops for low-power and high-performance systems. IEEE Transactions on very large scale integration (VLSI) systems, 14(12), 1379-1383. https://doi.org/10.1109/TVLSI.2006.887833

[15] Nagarajan, P., Saravanan, R., Thirumurugan, P. (2014). Design of register element for low power clocking system. Information: an international Interdisciplinary journal, 17(6), 2903-2913.

[16] Absel, K., Manuel, L., Kavitha, R.K. (2012). Low-power dual dynamic node pulsed hybrid flip-flop featuring efficient embedded logic. IEEE transactions on very large scale integration (vlsi) systems, 21(9), 1693-1704. https://doi.org/10.1109/TVLSI.2012.2213280

[17] John, P., Uyemura (2005). CMOS logic circuit design, Springer International edition.

[18] Rabaey, J.M, Pedram, M. (1996). Low Power Design Methodologies. Springer Science & Business Media, 366.

[19] Hodges, D., Jackson, H., & Saleh, R. (2003). Analysis and design of digital integrated circuits. McGraw-Hill, Inc.

[20] Gonzalez, R., Gorden, B.M., Horowitz, M. (1997). Supply and Threshold Voltage Scaling for Low Power CMOS', IEEE J. Solid state circuits, 32(8),1210-1216. https://doi.org/10.1109/4.604077

[21] Sengupta, D., Saleh, R. (2005). Power-delay metrics revisited for 90 nm CMOS technology. In Sixth international symposium on quality electronic design (isqed'05), IEEE, 291-296.

Conflict of interest: The Author have no conflicts of interest to declare that they are relevant to the content of this article.